FIG. 1A

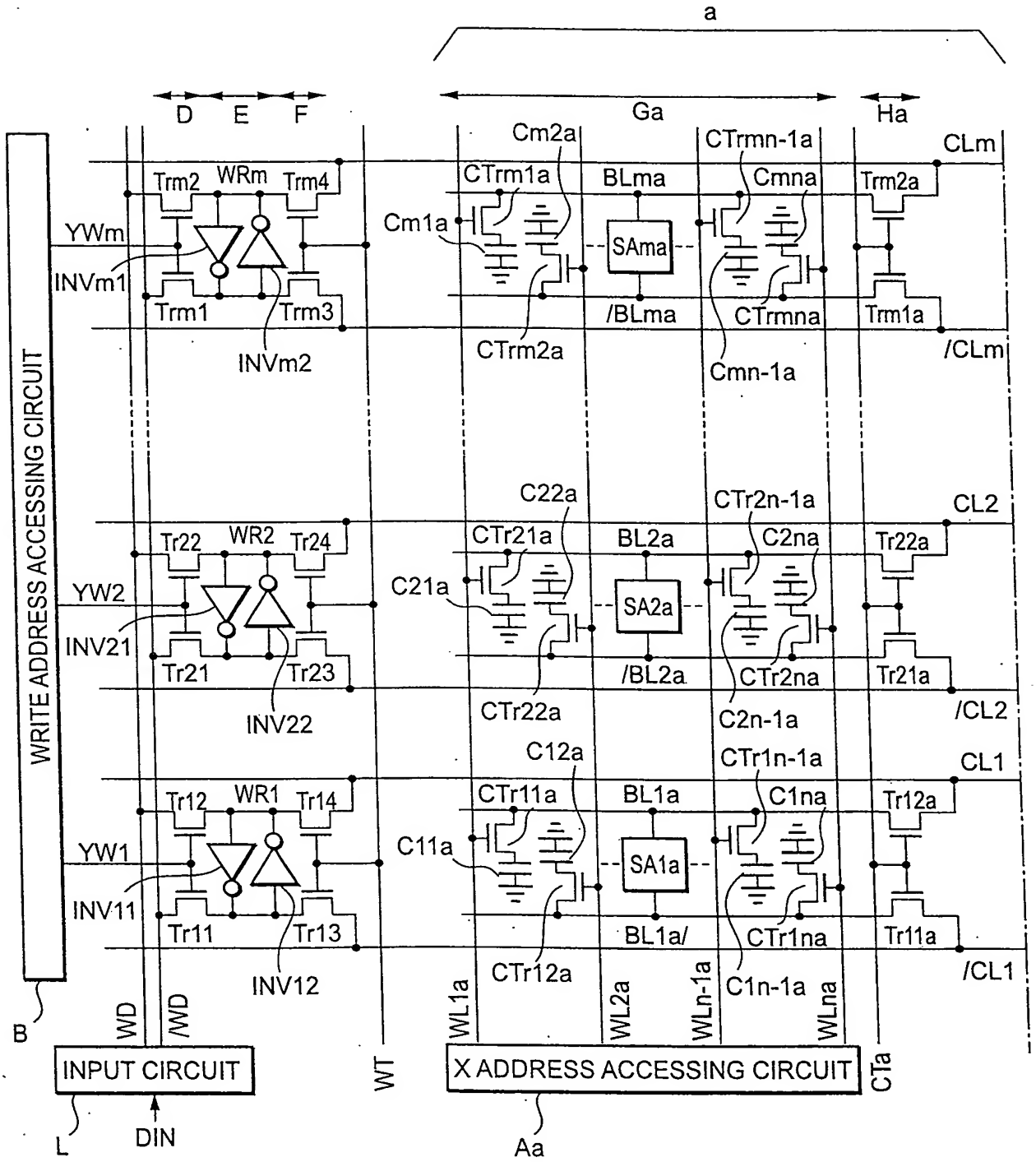

a
D
E
F
Ga
Ha
WRITE ADDRESS ACCESSING CIRCUIT
Trm2
WRm
Trm4
YWm
INVm1
Trm1
Trm3
INVm2
Cm2a
CTrm1a
BLma
CTrmn-1a
CLm
Cm1a
SAma
Cmna
Trm2a
/BLma
CTrmna
Trm1a
CTrm2a
Cmn-1a
/CLm
C22a
CTr2n-1a
CL2
Tr22
WR2
Tr24
CTr21a
BL2a
C2na
Tr22a
YW2
C21a
SA2a
INV21
Tr21
Tr23
/BL2a
CTr2na
Tr21a
INV22
CTr22a
C2n-1a
/CL2
C12a
CTr1n-1a
CL1
Tr12
WR1
Tr14
CTr11a
BL1a
C1na
Tr12a
YW1
C11a
SA1a
INV11
Tr11
Tr13
BL1a/
CTr1na
Tr11a
INV12
CTr12a
C1n-1a
/CL1
B
WD
/WD
WL1a
WL2a
WLn-1a
WLna
WT
CTa
INPUT CIRCUIT
X ADDRESS ACCESSING CIRCUIT
L
DIN
Aa

FIG. 1B

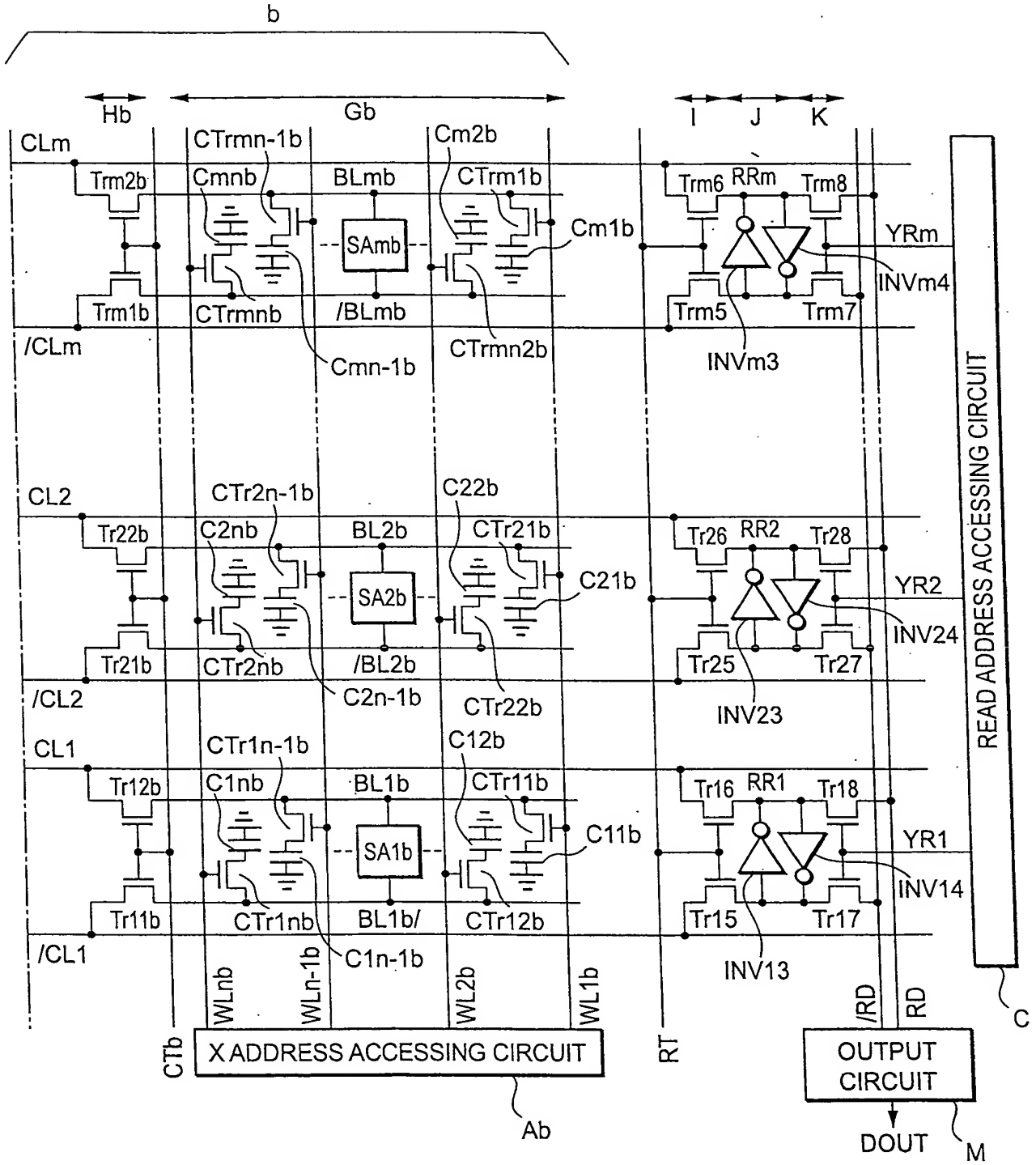

b
Hb
Gb
I
J
K
CLm
/CLm
CL2
/CL2
CL1
/CL1
Trm2b
Trm1b
Tr22b
Tr21b
Tr12b
Tr11b
CTrmn-1b
Cmnb
CTrmnb
Cmn-1b
BLmb
/BLmb
SAmb
Cm2b
CTrm1b
CTrmn2b
Cm1b
CTr2n-1b
C2nb
CTr2nb
C2n-1b
BL2b
/BL2b
SA2b
C22b
CTr21b
CTr22b
C21b
CTr1n-1b
C1nb
CTr1nb
C1n-1b
BL1b
BL1b/
SA1b
C12b
CTr11b
CTr12b
C11b
Trm6
RRm
Trm8
Trm5
Trm7
INVm3
INVm4
YRm
Tr26
RR2
Tr28
Tr25
Tr27
INV23
INV24
YR2
Tr16
RR1
Tr18
Tr15
Tr17
INV13
INV14
YR1
READ ADDRESS ACCESSING CIRCUIT
C
WLnb
WLn-1b
WL2b
WL1b
CTb
X ADDRESS ACCESSING CIRCUIT
Ab
RT
/RD
RD
OUTPUT CIRCUIT
DOUT
M

FIG. 2

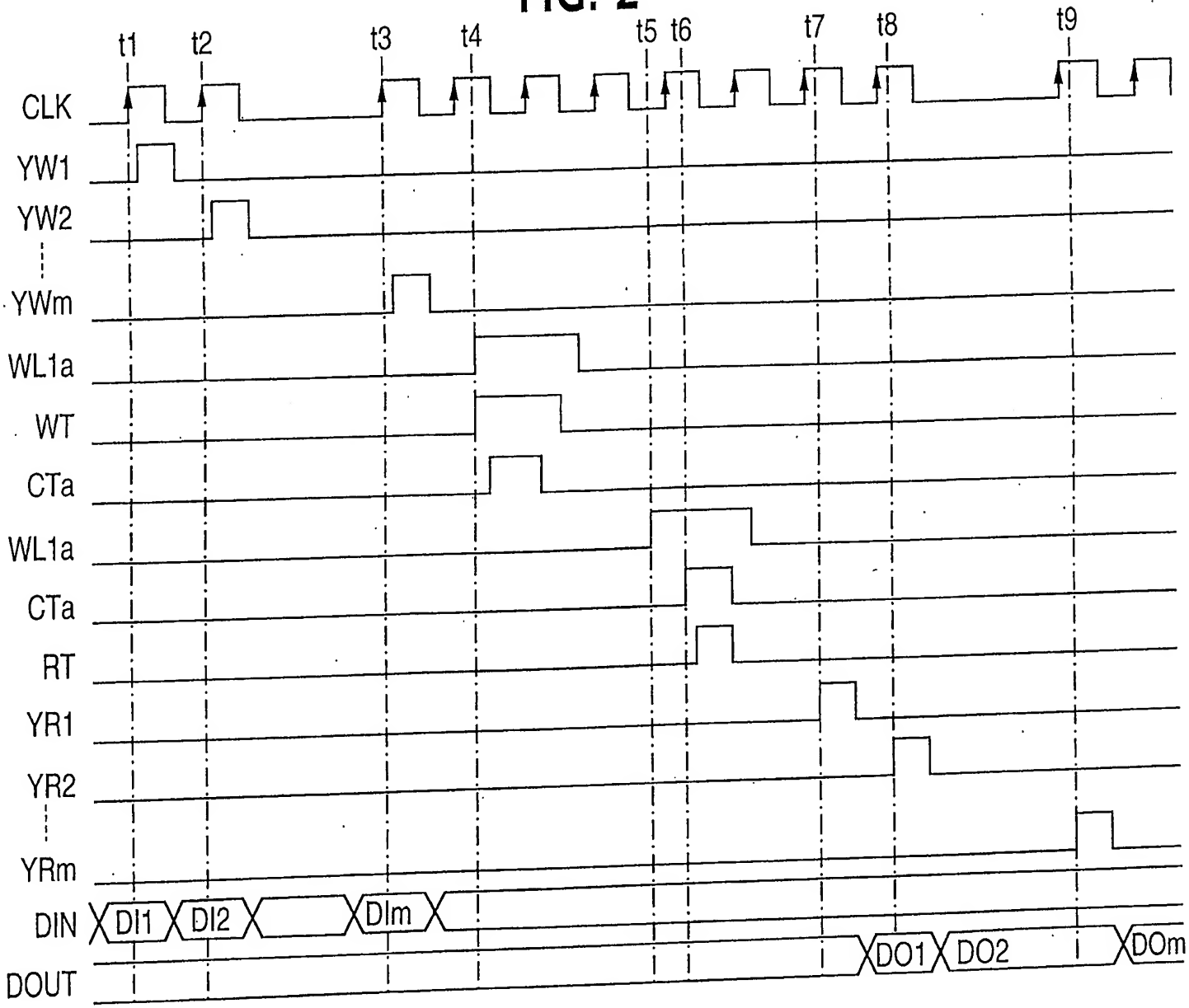

t1
t2
t3
t4
t5
t6
t7
t8
t9
CLK
YW1
YW2
YWm
WL1a
WT
CTa
WL1a
CTa
RT
YR1
YR2
YRm
DIN
DI1
DI2
DIm
DOUT
DO1
DO2
DOm

FIG. 3A

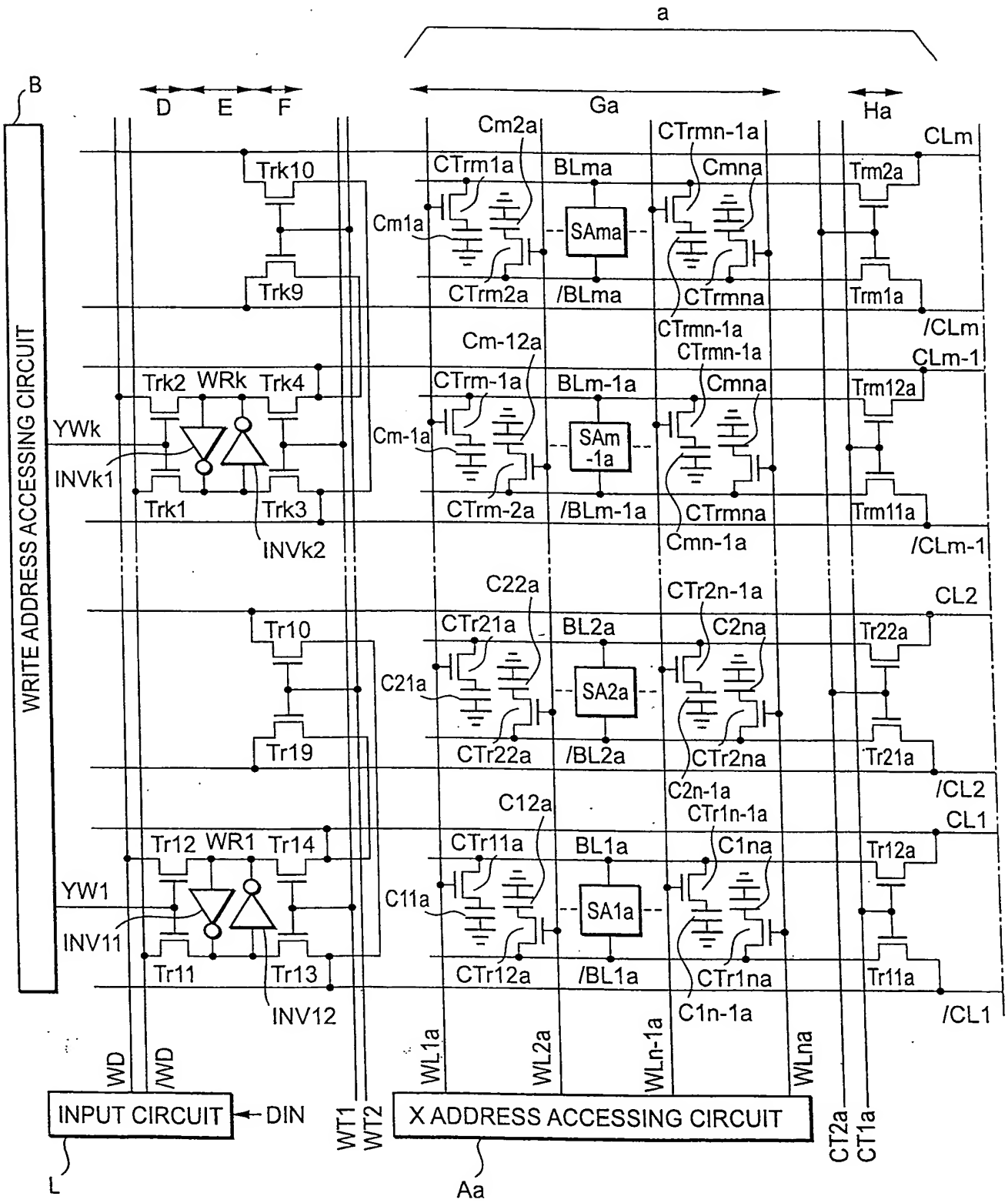

a
B
D
E
F
Ga
Ha
WRITE ADDRESS ACCESSING CIRCUIT
Trk10
Trk9
Trk2
WRk
Trk4
YWk
INVk1
Trk1
Trk3
INVk2
Tr10
Tr19
Tr12
WR1
Tr14
YW1
INV11
Tr11
Tr13
INV12
Cm2a
CTrm1a
BLma
Cm1a
SAma
CTrm2a
/BLma
CTrmn-1a
Cmna
CTrmna
Cm-12a
CTrm-1a
BLm-1a
Cm-1a
SAm
-1a
CTrm-2a
/BLm-1a
Cmn-1a
C22a
CTr21a
BL2a
C21a
SA2a
CTr22a
/BL2a
CTr2n-1a
C2na
CTr2na
C2n-1a
C12a
CTr11a
BL1a
C11a
SA1a
CTr12a
/BL1a
CTr1n-1a
C1na
CTr1na
C1n-1a
CLm
Trm2a
Trm1a
/CLm
CLm-1
Trm12a
Trm11a
/CLm-1
CL2
Tr22a
Tr21a
/CL2
CL1
Tr12a
Tr11a
/CL1
WD
/WD
INPUT CIRCUIT
DIN
L
WT1
WT2
WL1a
WL2a
WLn-1a
WLna
X ADDRESS ACCESSING CIRCUIT
Aa
CT2a
CT1a

FIG.3B

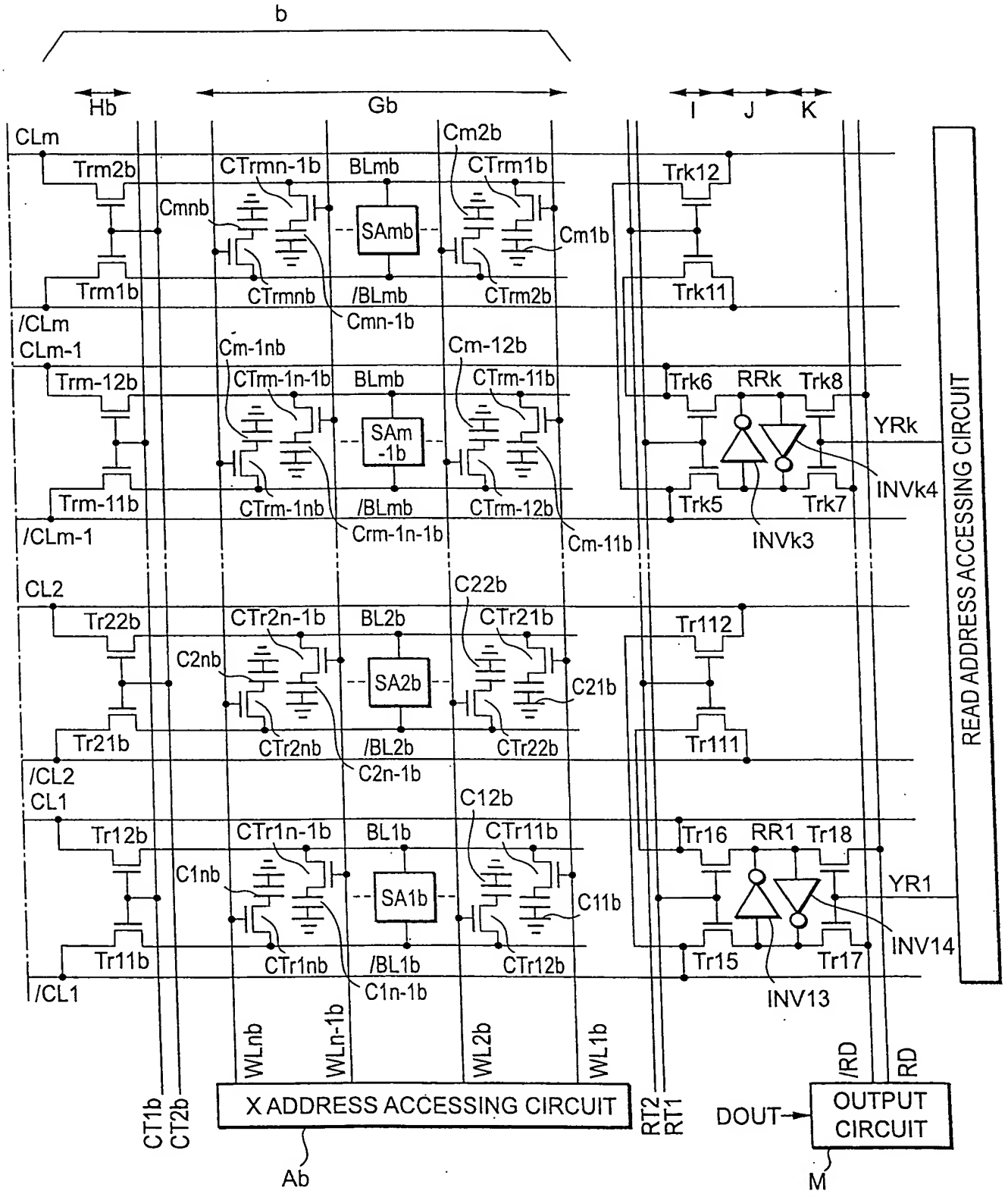

b
Hb
Gb
I
J
K
CLm
Trm2b
CTrmn-1b
BLmb
Cm2b
CTrm1b
Trk12
Cmnb
SAmb
Cm1b
Trm1b
CTrmnb
/BLmb
CTrm2b
Trk11
Cmn-1b
/CLm
CLm-1
Cm-1nb
Cm-12b
Trm-12b
CTrm-1n-1b
BLmb
CTrm-11b
Trk6
RRk
Trk8
YRk
SAm
-1b
Trm-11b
CTrm-1nb
/BLmb
CTrm-12b
Trk5
Trk7
INVk4
/CLm-1
Crm-1n-1b
Cm-11b
INVk3
CL2
C22b
Tr22b
CTr2n-1b
BL2b
CTr21b
Tr112
C2nb
SA2b
C21b
Tr21b
CTr2nb
/BL2b
CTr22b
Tr111
/CL2
C2n-1b
CL1
C12b
Tr12b
CTr1n-1b
BL1b
CTr11b
Tr16
RR1
Tr18
C1nb
SA1b
C11b
YR1
Tr11b
CTr1nb
/BL1b
CTr12b
Tr15
Tr17
INV14
/CL1
C1n-1b
INV13
READ ADDRESS ACCESSING CIRCUIT
WLnb
WLn-1b
WL2b
WL1b
/RD
RD
CT1b
CT2b
X ADDRESS ACCESSING CIRCUIT
RT2
RT1
DOUT
OUTPUT CIRCUIT
Ab
M

FIG. 4

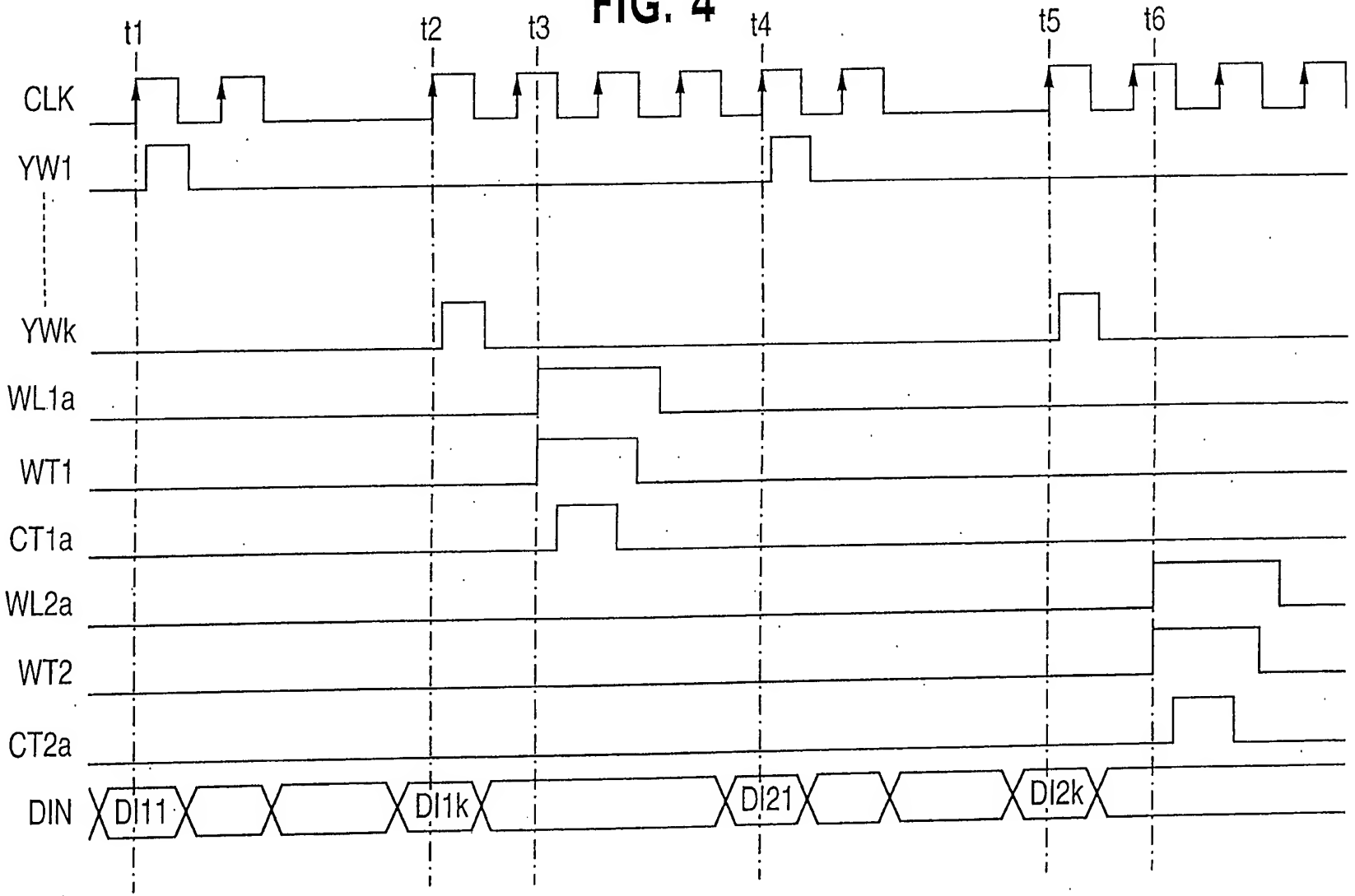

t1
t2
t3
t4
t5
t6
CLK
YW1
YWk
WL1a
WT1
CT1a
WL2a
WT2
CT2a
DIN
DI11
DI1k
DI21
DI2k

FIG.5A

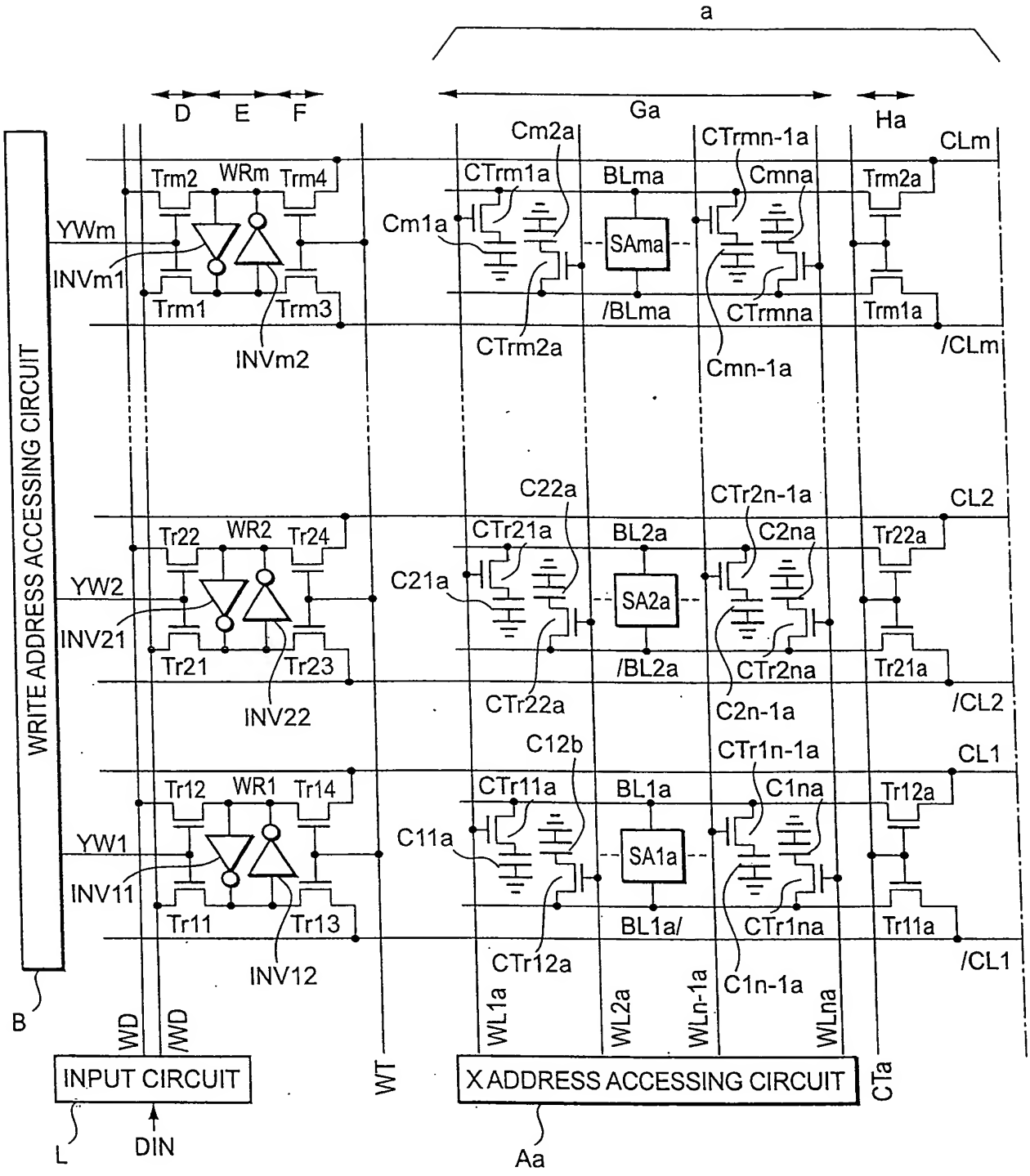

a
D
E
F
Ga
Ha
WRITE ADDRESS ACCESSING CIRCUIT
YWm
YW2
YW1
INVm1
INV21
INV11
Trm2
WRm
Trm4
Trm1
Trm3
INVm2
Tr22
WR2
Tr24
Tr21
Tr23
INV22
Tr12
WR1
Tr14
Tr11
Tr13
INV12
Cm2a
CTrm1a
BLma
Cmna
CTrmn-1a
Cm1a
SAma
/BLma
CTrmna
CTrm2a
Cmn-1a
C22a
CTr21a
BL2a
C2na
CTr2n-1a
C21a
SA2a
/BL2a
CTr2na
CTr22a
C2n-1a
C12b
CTr11a
BL1a
C1na
CTr1n-1a
C11a
SA1a
BL1a/
CTr1na
CTr12a
C1n-1a
Trm2a
Trm1a
Tr22a
Tr21a
Tr12a
Tr11a
CLm
/CLm
CL2
/CL2
CL1
/CL1
B
WD
/WD
WT
WL1a
WL2a
WLn-1a
WLna
CTa
INPUT CIRCUIT
X ADDRESS ACCESSING CIRCUIT
L
DIN
Aa

FIG.5B

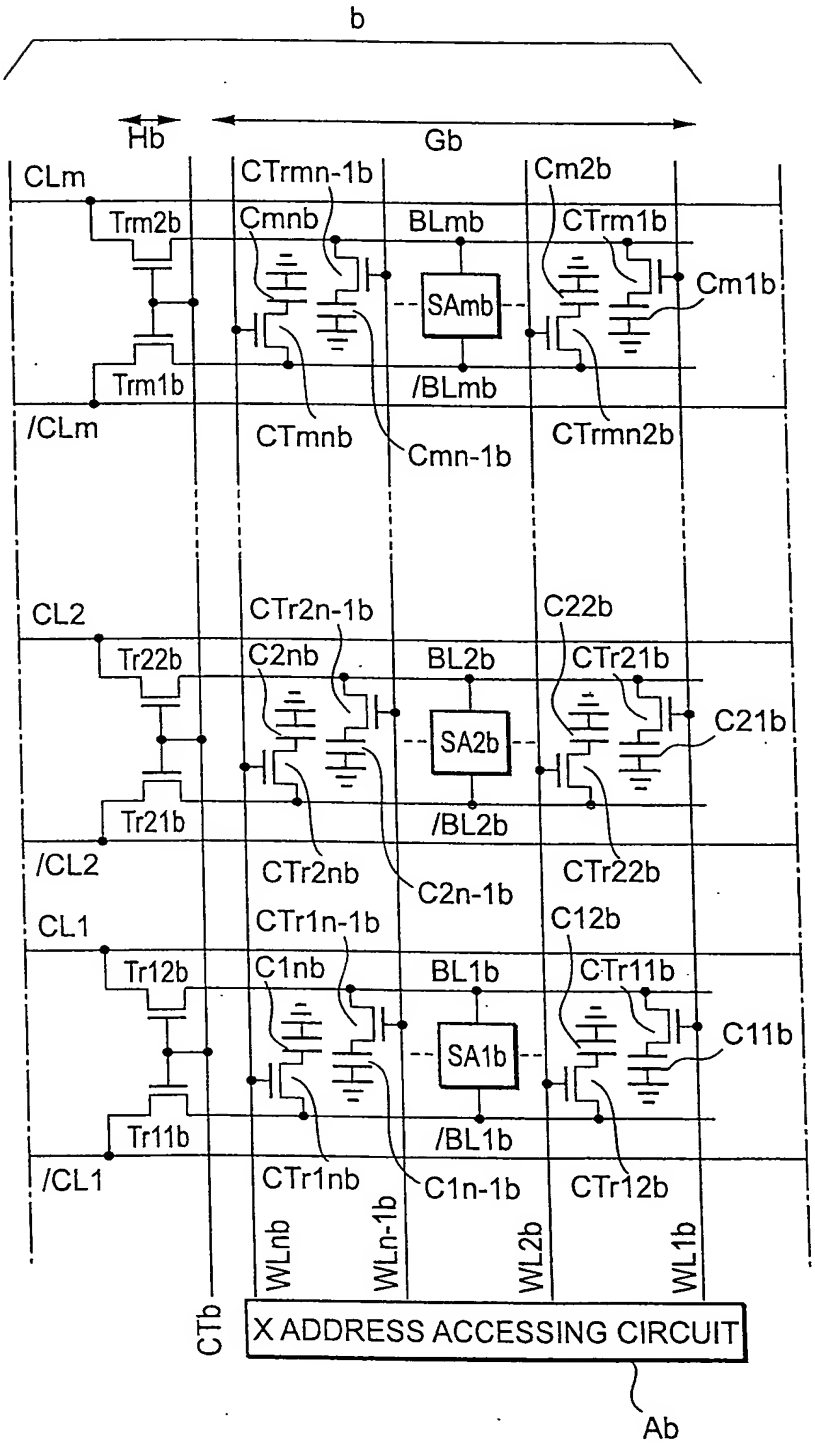

b
Hb
Gb
CLm
Trm2b
Trm1b
/CLm
CTrmn-1b
Cmnb
CTmnb
Cmn-1b
BLmb
SAmb
/BLmb
Cm2b
CTrm1b
Cm1b
CTrmn2b
CL2
Tr22b
Tr21b
/CL2
CTr2n-1b
C2nb
CTr2nb
C2n-1b
BL2b
SA2b
/BL2b
C22b
CTr21b
C21b
CTr22b
CL1
Tr12b
Tr11b
/CL1
CTr1n-1b
C1nb
CTr1nb
C1n-1b
BL1b
SA1b
/BL1b
C12b
CTr11b
C11b
CTr12b
WLnb
WLn-1b
WL2b
WL1b
CTb
X ADDRESS ACCESSING CIRCUIT
Ab

FIG.5C

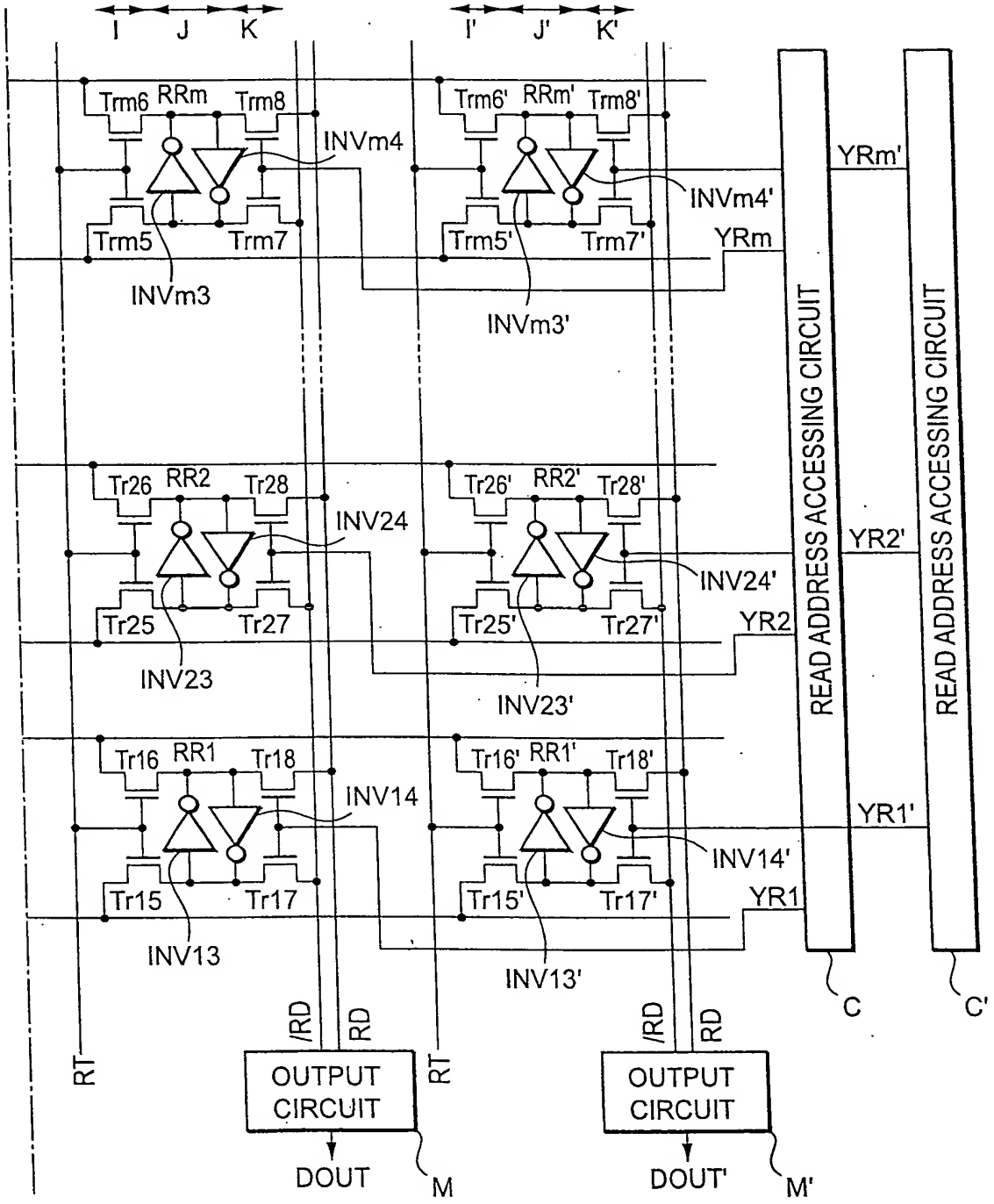

I
J
K
I'
J'
K'
Trm6
RRm
Trm8
INVm4
Trm5
Trm7
INVm3
Trm6'
RRm'
Trm8'
INVm4'
Trm5'
Trm7'
INVm3'
YRm'
YRm
READ ADDRESS ACCESSING CIRCUIT
READ ADDRESS ACCESSING CIRCUIT
Tr26
RR2
Tr28
INV24
Tr25
Tr27
INV23
Tr26'
RR2'
Tr28'
INV24'
Tr25'
Tr27'
INV23'
YR2'
YR2
Tr16
RR1
Tr18
INV14
Tr15
Tr17
INV13
Tr16'
RR1'
Tr18'
INV14'
Tr15'
Tr17'
INV13'
YR1'
YR1
C
C'
RT
/RD
RD
OUTPUT CIRCUIT
DOUT
M
RT
/RD
RD
OUTPUT CIRCUIT
DOUT'
M'

FIG. 6

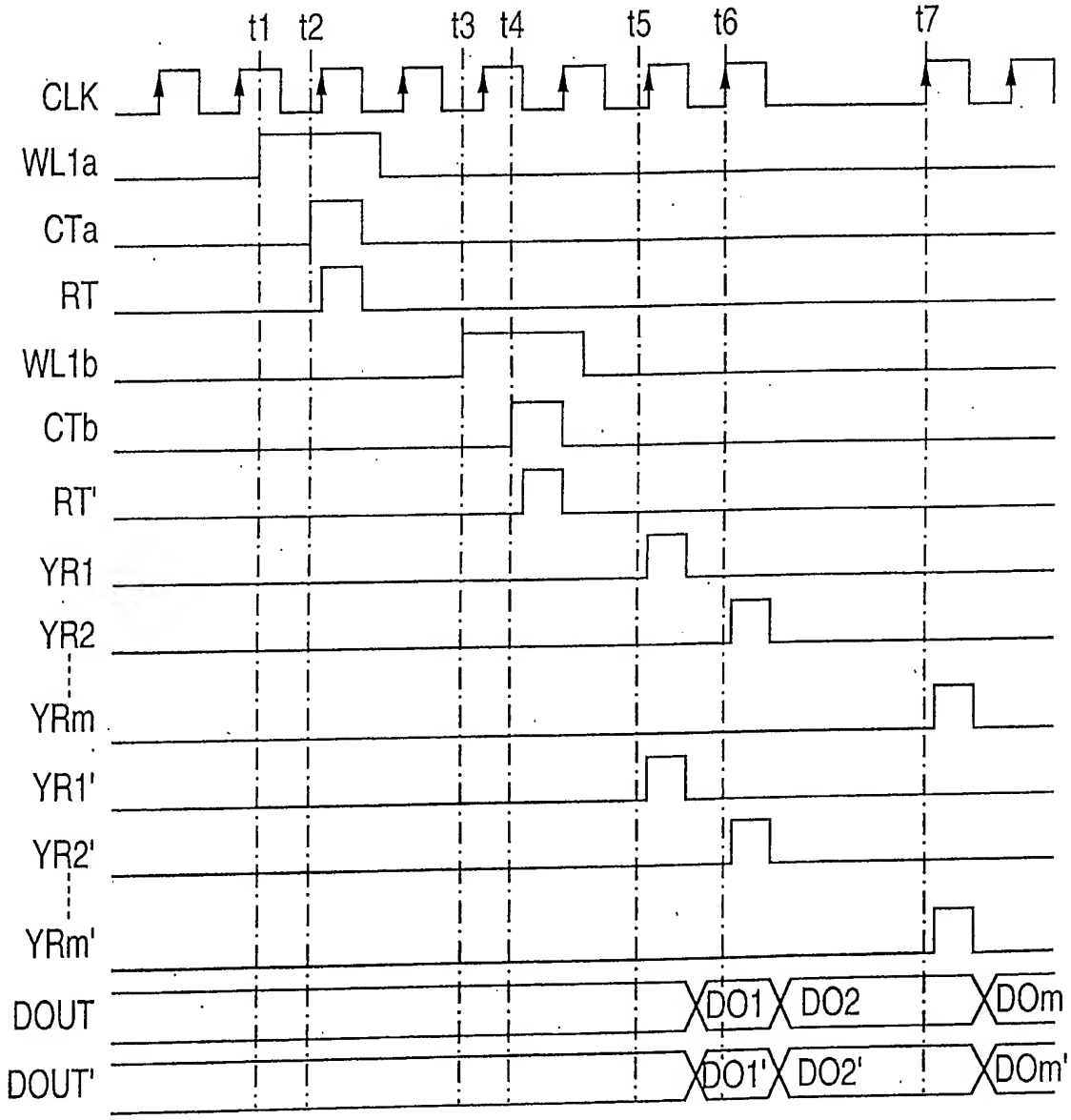

t1
t2
t3
t4
t5
t6
t7
CLK
WL1a
CTa
RT
WL1b
CTb
RT'
YR1
YR2
YRm
YR1'
YR2'
YRm'
DOUT
DO1
DO2
DOm
DOUT'
DO1'
DO2'
DOm'

FIG.7A

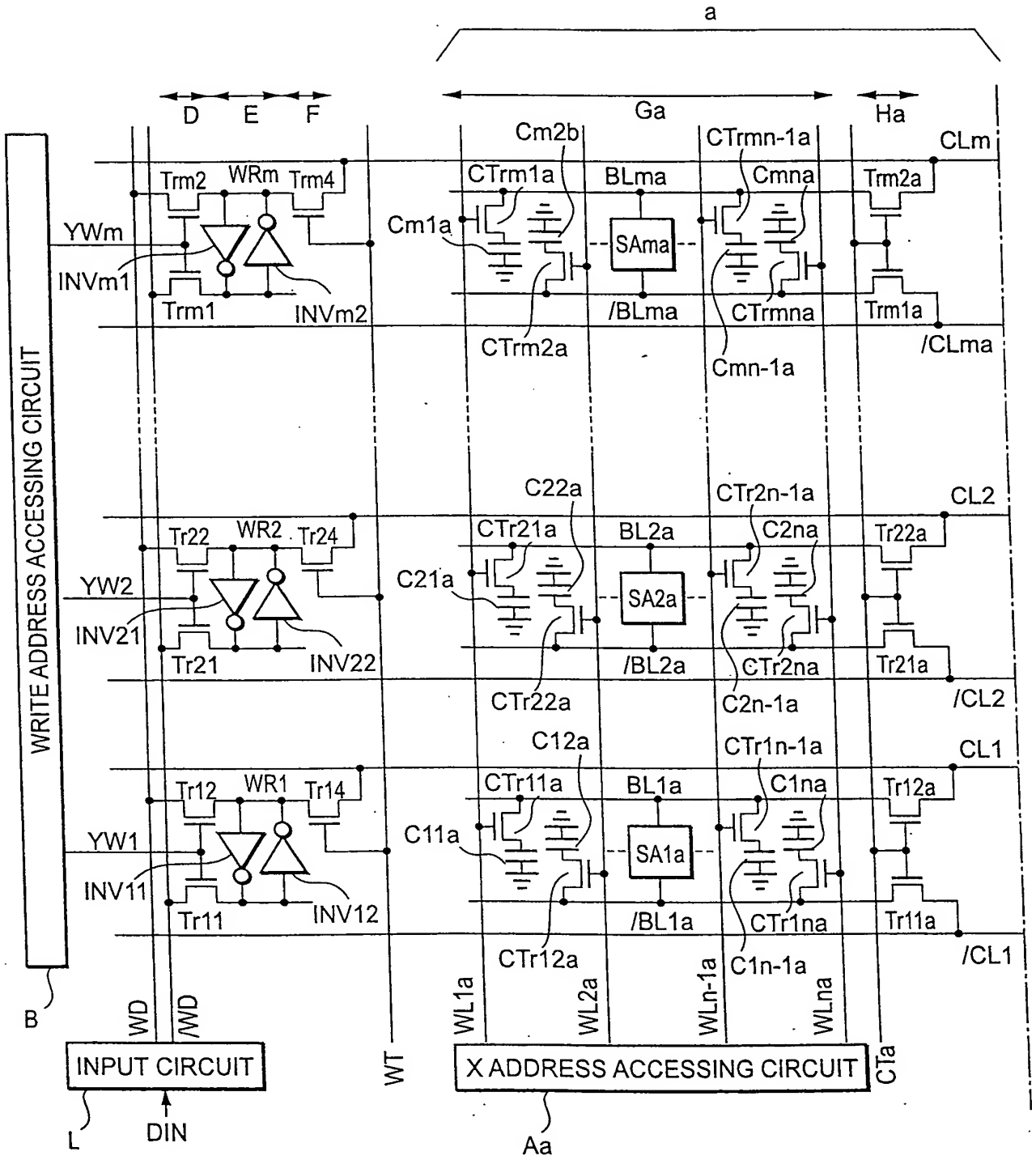

a
D
E
F
Ga
Ha
WRITE ADDRESS ACCESSING CIRCUIT
Trm2
WRm
Trm4
YWm
INVm1
Trm1
INVm2
Cm2b
CTrm1a
BLma
CTrmn-1a
CLm
Cm1a
SAma
Cmna
Trm2a
/BLma
CTrmna
Trm1a
CTrm2a
Cmn-1a
/CLma
C22a
CTr2n-1a
CL2
Tr22
WR2
Tr24
CTr21a
BL2a
Tr22a
YW2
C21a
SA2a
C2na
INV21
Tr21
INV22
/BL2a
CTr2na
Tr21a
CTr22a
C2n-1a
/CL2
C12a
CTr1n-1a
CL1
Tr12
WR1
Tr14
CTr11a
BL1a
C1na
Tr12a
YW1
C11a
SA1a
INV11
Tr11
INV12
/BL1a
CTr1na
Tr11a
CTr12a
C1n-1a
/CL1
B
WD
/WD
WL1a
WL2a
WLn-1a
WLna
WT
CTa
INPUT CIRCUIT
X ADDRESS ACCESSING CIRCUIT
L
DIN
Aa

FIG.7B

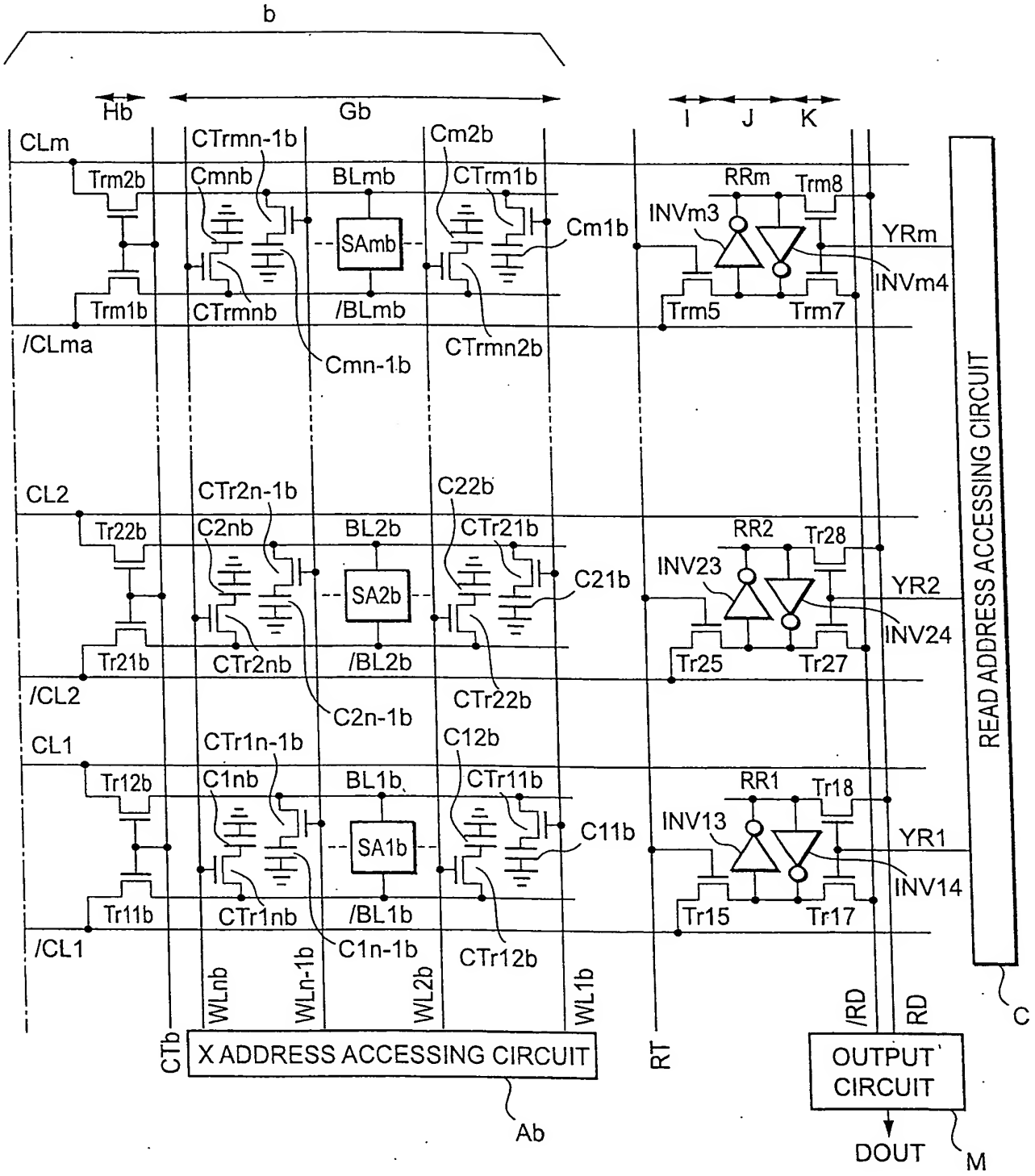

b
Hb
Gb
I
J
K
CLm
CTrmn-1b
Cm2b
Trm2b
Cmnb
BLmb
CTrm1b
RRm
Trm8
INVm3
Cm1b
SAmb
YRm
INVm4
Trm1b
CTrmnb
/BLmb
Trm5
Trm7
/CLma
Cmn-1b
CTrmn2b
READ ADDRESS ACCESSING CIRCUIT
CL2
CTr2n-1b
C22b
Tr22b
C2nb
BL2b
CTr21b
RR2
Tr28
INV23
C21b
SA2b
YR2
INV24
Tr21b
CTr2nb
/BL2b
Tr25
Tr27
/CL2
C2n-1b
CTr22b
CL1
CTr1n-1b
C12b
Tr12b
C1nb
BL1b
CTr11b
RR1
Tr18
INV13
C11b
SA1b
YR1
INV14
Tr11b
CTr1nb
/BL1b
Tr15
Tr17
/CL1
C1n-1b
CTr12b
WLnb
WLn-1b
WL2b
WL1b
/RD
RD
C
CTb
X ADDRESS ACCESSING CIRCUIT
RT
OUTPUT CIRCUIT
Ab
DOUT
M

FIG.8A

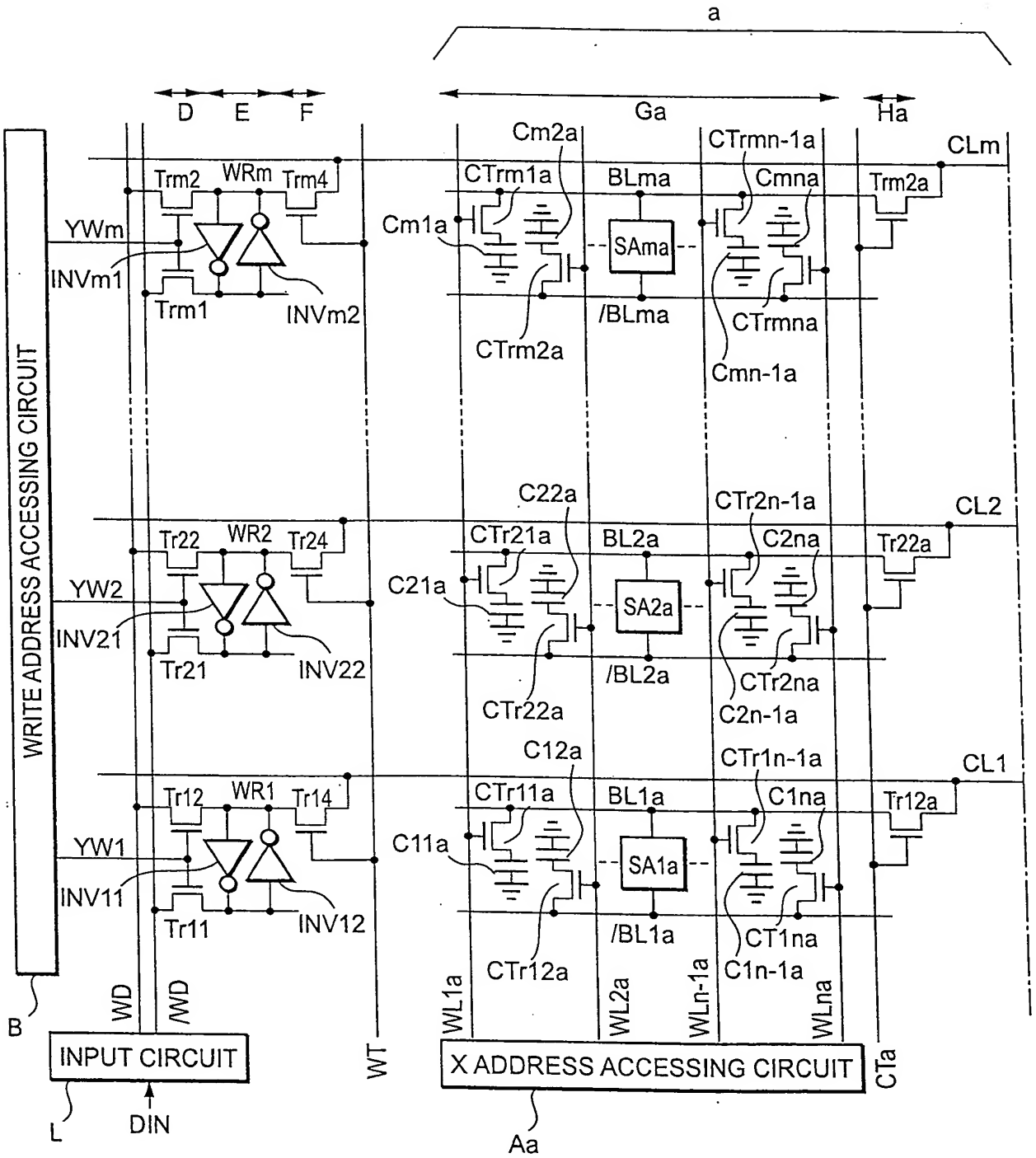

a
D
E
F
Ga
Ha
WRITE ADDRESS ACCESSING CIRCUIT
Trm2
WRm
Trm4
YWm
INVm1
Trm1
INVm2
Cm2a
CTrm1a
BLma
CTrmn-1a
CLm
Cm1a
SAma
Cmna
Trm2a
/BLma
CTrmna
CTrm2a
Cmn-1a
C22a
CTr21a
BL2a
CTr2n-1a
CL2
Tr22
WR2
Tr24
YW2
INV21
Tr21
INV22
C21a
SA2a
C2na
Tr22a
/BL2a
CTr2na
CTr22a
C2n-1a
C12a
CTr11a
BL1a
CTr1n-1a
CL1
Tr12
WR1
Tr14
YW1
INV11
Tr11
INV12
C11a
SA1a
C1na
Tr12a
/BL1a
CT1na
CTr12a
C1n-1a
WL1a
WL2a
WLn-1a
WLna
B
WD
/WD
WT
CTa
INPUT CIRCUIT
X ADDRESS ACCESSING CIRCUIT
L
DIN
Aa

FIG.8B

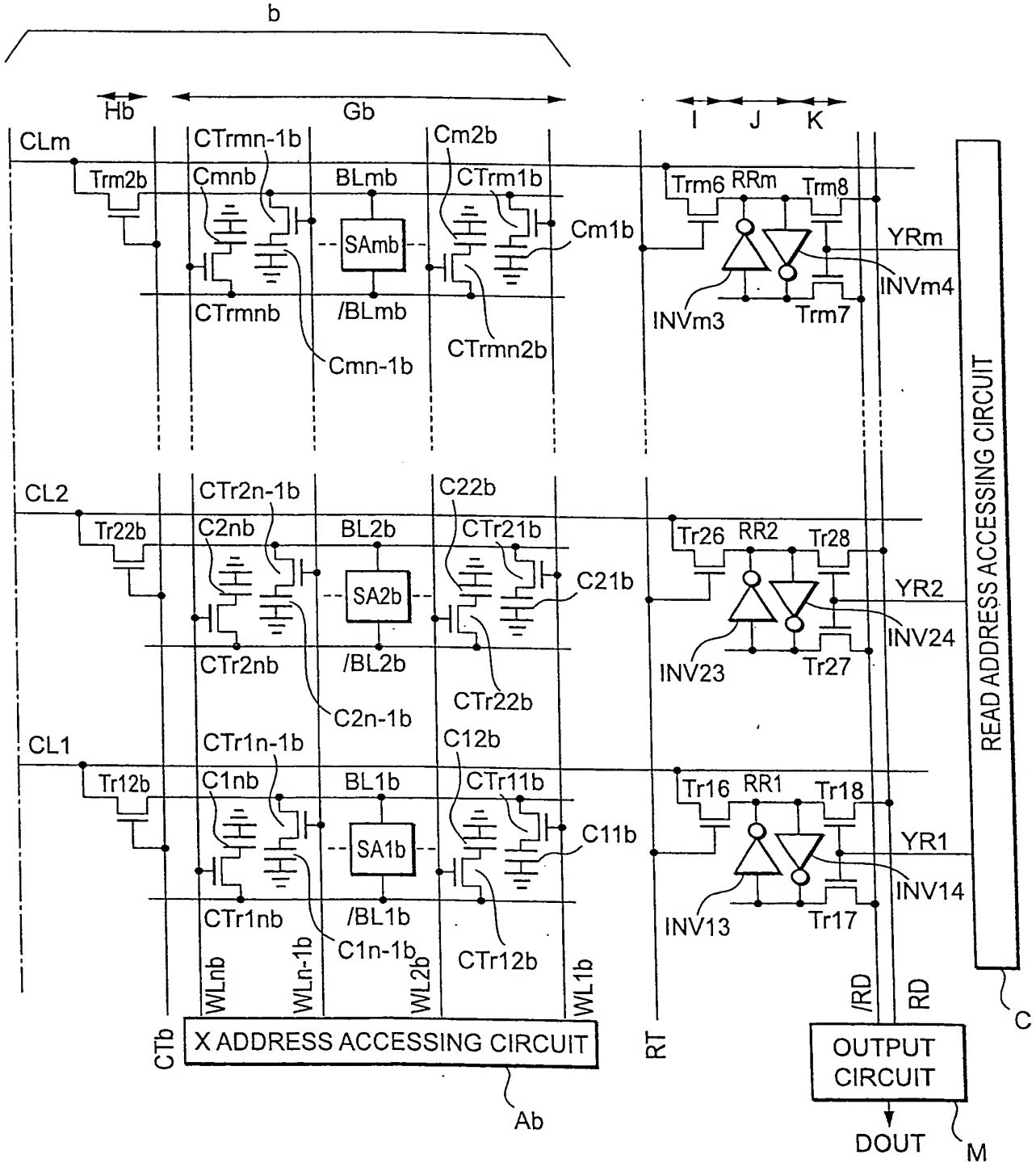

b
Hb
Gb
I
J
K
CLm
Trm2b
CTrmn-1b
Cmnb
BLmb
Cm2b
CTrm1b
Trm6
RRm
Trm8
SAmb
Cm1b
YRm
INVm4
CTrmnb
/BLmb
INVm3
Trm7
Cmn-1b
CTrmn2b
CL2
Tr22b
CTr2n-1b
C2nb
BL2b
C22b
CTr21b
Tr26
RR2
Tr28
SA2b
C21b
YR2
INV24
CTr2nb
/BL2b
INV23
Tr27
C2n-1b
CTr22b
CL1
Tr12b
CTr1n-1b
C1nb
BL1b
C12b
CTr11b
Tr16
RR1
Tr18
SA1b
C11b
YR1
INV14
CTr1nb
/BL1b
INV13
Tr17
C1n-1b
CTr12b
READ ADDRESS ACCESSING CIRCUIT
WLnb
WLn-1b
WL2b
WL1b
/RD
RD
C
CTb
X ADDRESS ACCESSING CIRCUIT
RT
OUTPUT CIRCUIT
Ab
DOUT
M

FIG.9A

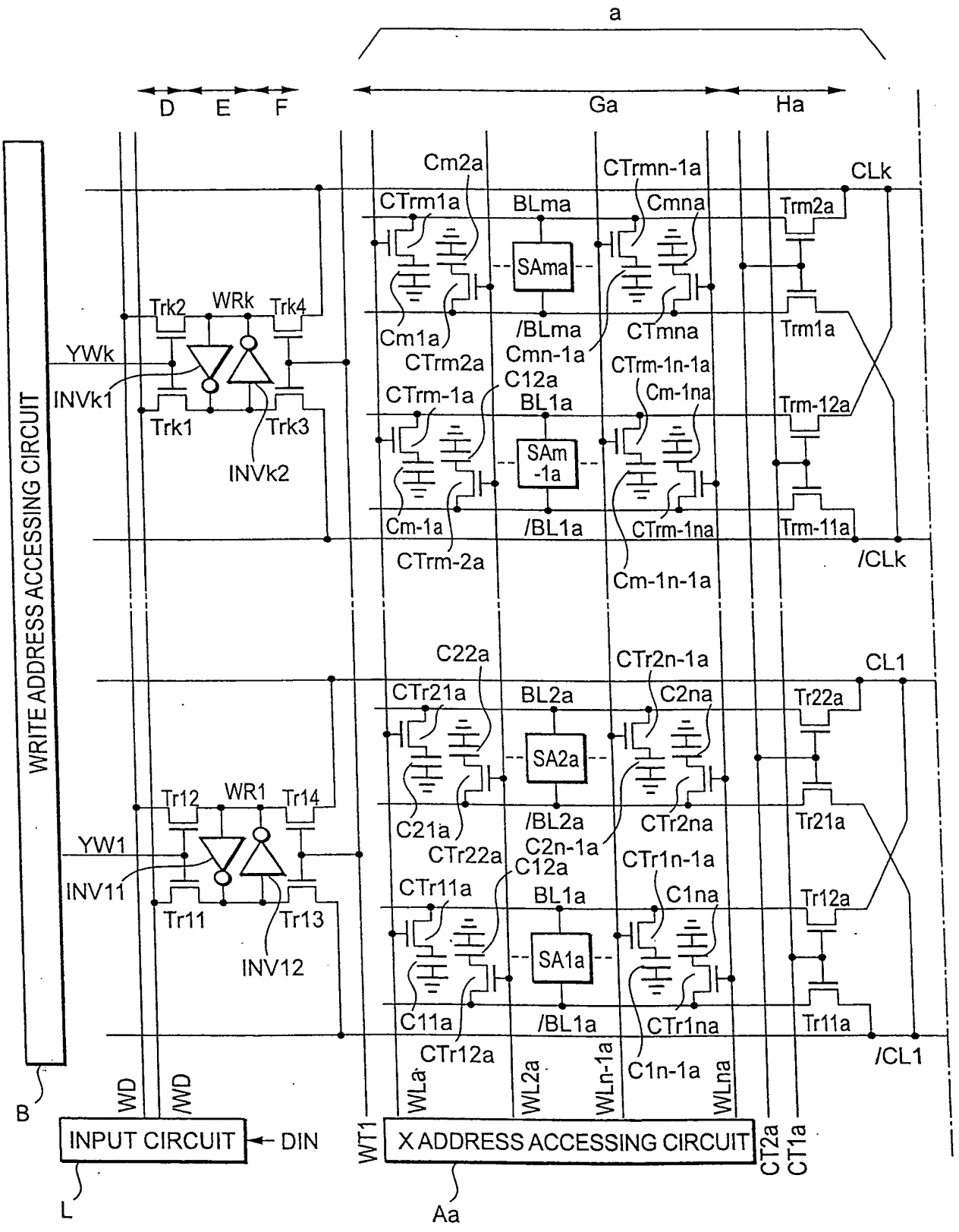

a
D
E
F
Ga
Ha
WRITE ADDRESS ACCESSING CIRCUIT
Cm2a
CTrmn-1a
CLk
CTrm1a
BLma
Cmna
Trm2a
SAma
Trk2
WRk
Trk4
Cm1a
/BLma
CTmna
Trm1a
YWk
CTrm2a
Cmn-1a
CTrm-1n-1a
INVk1
C12a
CTrm-1a
BL1a
Cm-1na
Trm-12a
Trk1
Trk3
SAm
-1a
INVk2
Cm-1a
/BL1a
CTrm-1na
Trm-11a
CTrm-2a
/CLk
Cm-1n-1a
C22a
CTr2n-1a
CL1
CTr21a
BL2a
C2na
Tr22a
SA2a
Tr12
WR1
Tr14
C21a
/BL2a
CTr2na
Tr21a
YW1
CTr22a
C2n-1a
CTr1n-1a
C12a
INV11
CTr11a
BL1a
C1na
Tr12a
Tr11
Tr13
SA1a
INV12
C11a
/BL1a
CTr1na
Tr11a
CTr12a
/CL1
C1n-1a
B
WD
/WD
WLa
WL2a
WLn-1a
WLna
WT1
CT2a
CT1a
INPUT CIRCUIT
DIN
X ADDRESS ACCESSING CIRCUIT
L
Aa

FIG.9B

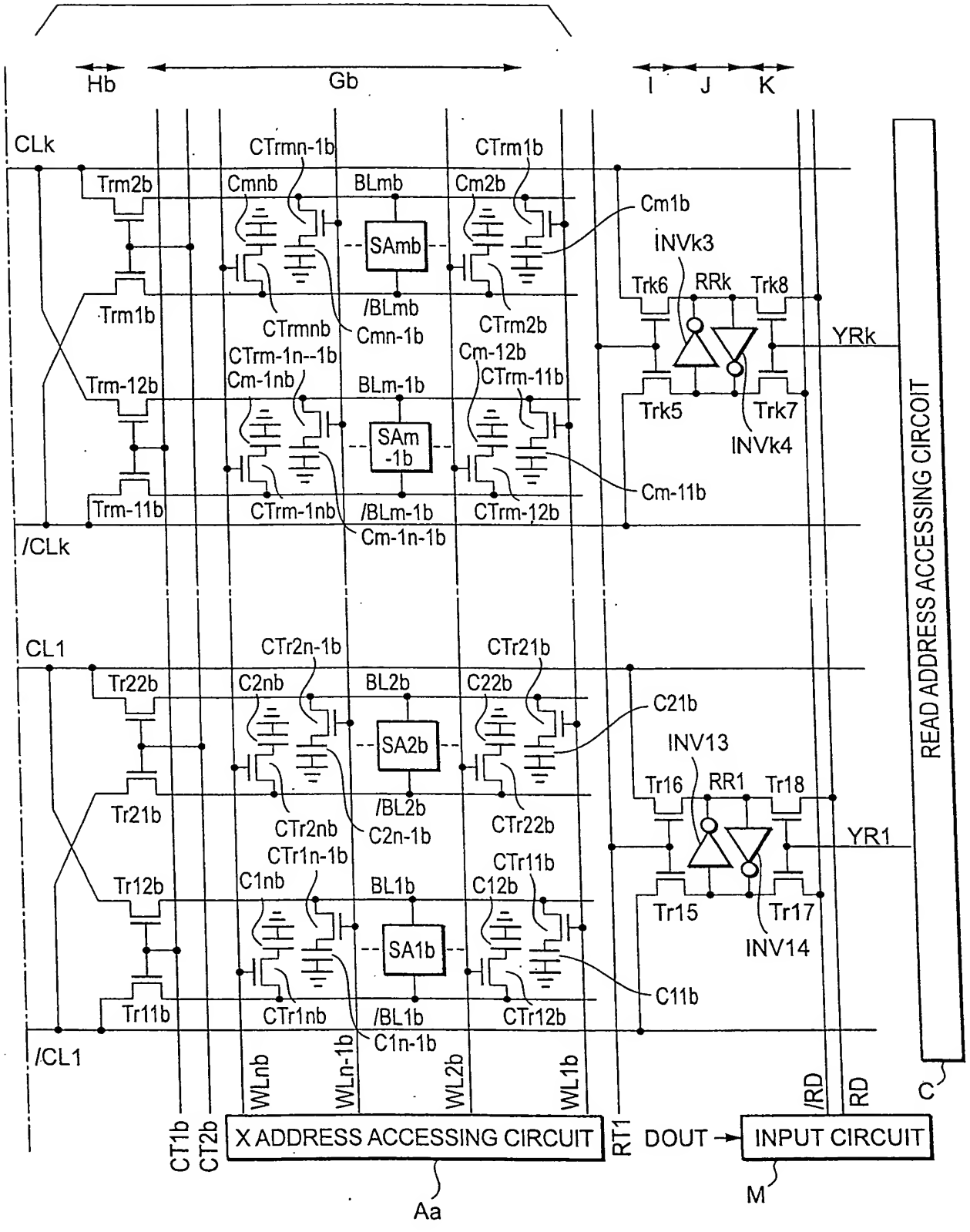

Hb
Gb
I
J
K
CLk
CTrmn-1b
CTrm1b
Trm2b
Cmnb
BLmb
Cm2b
Cm1b
SAmb
INVk3
Trk6
RRk
Trk8
Trm1b
/BLmb
CTrmnb
Cmn-1b
CTrm2b
YRk
CTrm-1n--1b
Cm-12b
Trm-12b
Cm-1nb
BLm-1b
CTrm-11b
Trk5
Trk7
SAm
-1b
INVk4
Cm-11b
Trm-11b
CTrm-1nb
/BLm-1b
CTrm-12b
Cm-1n-1b
/CLk
CL1
CTr2n-1b
CTr21b
Tr22b
C2nb
BL2b
C22b
C21b
SA2b
INV13
Tr16
RR1
Tr18
Tr21b
/BL2b
CTr2nb
C2n-1b
CTr22b
YR1
CTr1n-1b
CTr11b
Tr12b
C1nb
BL1b
C12b
Tr15
Tr17
SA1b
INV14
C11b
Tr11b
CTr1nb
/BL1b
CTr12b
C1n-1b
/CL1
WLnb
WLn-1b
WL2b
WL1b
/RD
RD
C
READ ADDRESS ACCESSING CIRCOIT
CT1b
CT2b
X ADDRESS ACCESSING CIRCUIT
RT1
DOUT
INPUT CIRCUIT
Aa
M

FIG.10A

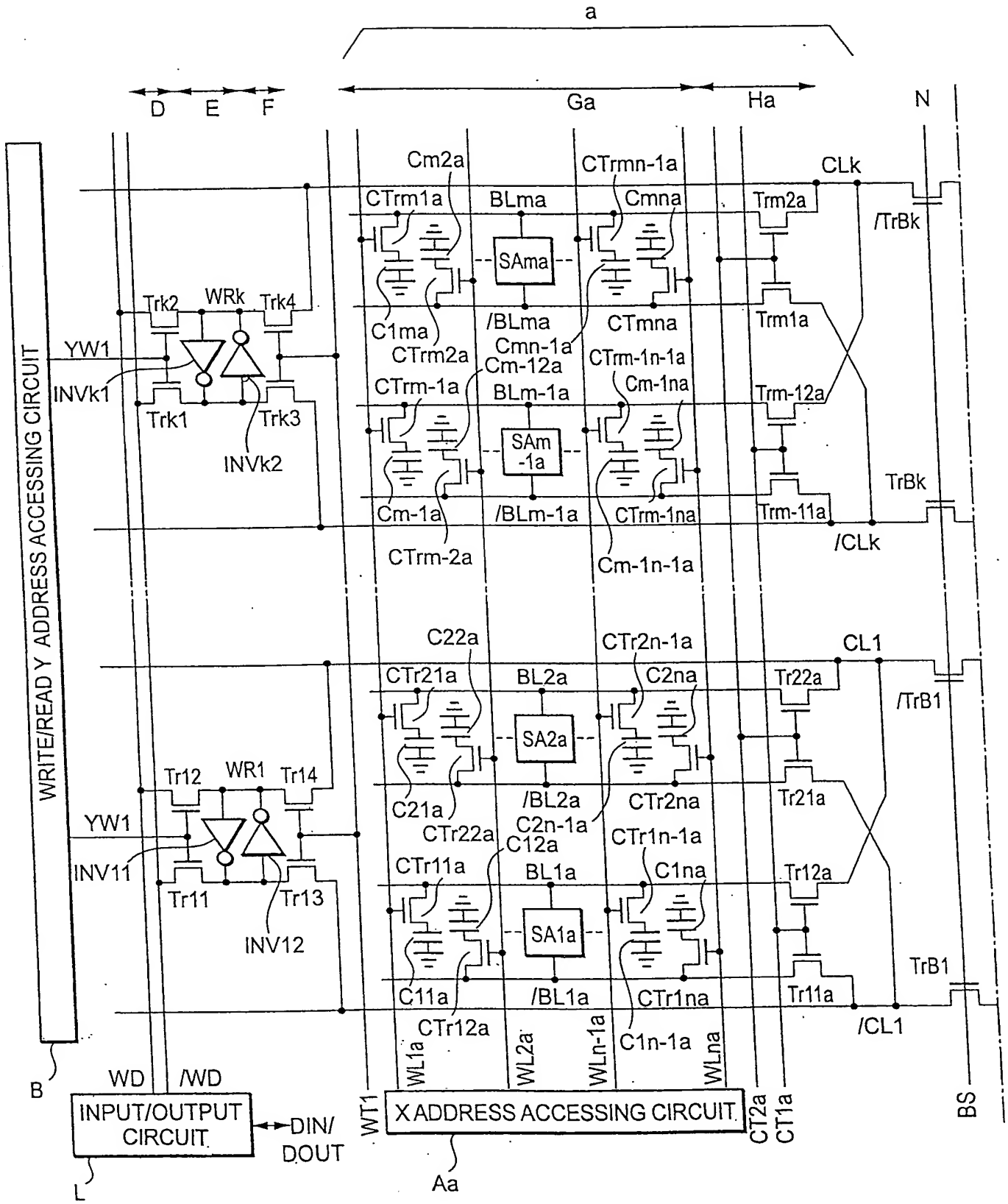

a
D
E
F
Ga
Ha
N
WRITE/READ Y ADDRESS ACCESSING CIRCUIT
Cm2a
CTrmn-1a
CLk
CTrm1a
BLma
Cmna
Trm2a
/TrBk
SAma
Trk2
WRk
Trk4
C1ma
/BLma
CTmna
Trm1a
YW1
CTrm2a
Cmn-1a
CTrm-1n-1a
INVk1
Cm-12a
CTrm-1a
BLm-1a
Cm-1na
Trm-12a
Trk1
Trk3
SAm
-1a
INVk2
TrBk
Cm-1a
/BLm-1a
CTrm-1na
Trm-11a
/CLk
CTrm-2a
Cm-1n-1a
C22a
CTr2n-1a
CL1
CTr21a
BL2a
C2na
Tr22a
/TrB1
SA2a
Tr12
WR1
Tr14
C21a
/BL2a
CTr2na
Tr21a
YW1
CTr22a
C2n-1a
CTr1n-1a
C12a
INV11
CTr11a
BL1a
C1na
Tr12a
Tr11
Tr13
SA1a
INV12
TrB1
C11a
/BL1a
CTr1na
Tr11a
CTr12a
/CL1
C1n-1a
WL1a
WL2a
WLn-1a
WLna
B
WD
/WD
WT1
CT2a
CT1a
BS
INPUT/OUTPUT
CIRCUIT
DIN/
DOUT
X ADDRESS ACCESSING CIRCUIT
L
Aa

FIG.10B

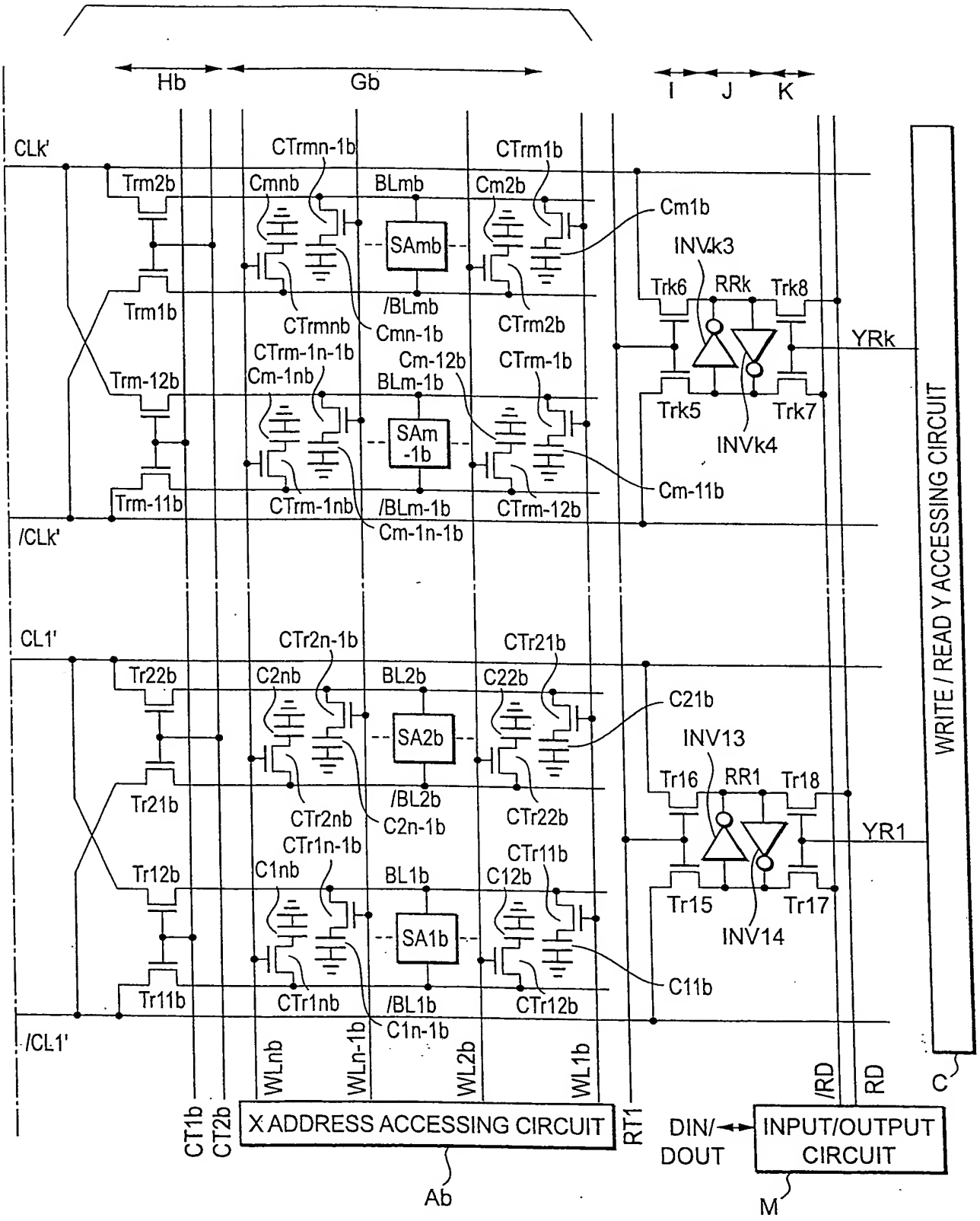

Hb
Gb
I
J
K
CLk'
/CLk'
CL1'
/CL1'
CTrmn-1b
CTrm1b
Trm2b
Cmnb
BLmb
Cm2b
Cm1b
SAmb
INVk3
Trk6
RRk
Trk8
/BLmb
Trm1b
CTrmnb
Cmn-1b
CTrm2b
YRk
CTrm-1n-1b
Cm-12b
CTrm-1b
Trm-12b
Cm-1nb
BLm-1b
SAm
-1b
Trk5
Trk7
INVk4
Cm-11b
Trm-11b
CTrm-1nb
/BLm-1b
CTrm-12b
Cm-1n-1b
CTr2n-1b
CTr21b
Tr22b
C2nb
BL2b
C22b
C21b
SA2b
INV13
Tr16
RR1
Tr18
/BL2b
Tr21b
CTr2nb
C2n-1b
CTr22b
YR1
CTr1n-1b
CTr11b
Tr12b
C1nb
BL1b
C12b
SA1b
Tr15
Tr17
INV14
C11b
Tr11b
CTr1nb
/BL1b
CTr12b
C1n-1b
WLnb
WLn-1b
WL2b
WL1b
/RD
RD
C
WRITE / READ Y ACCESSING CIRCUIT
CT1b
CT2b
X ADDRESS ACCESSING CIRCUIT
RT1
DIN/
DOUT
INPUT/OUTPUT
CIRCUIT
Ab
M

FIG.11A

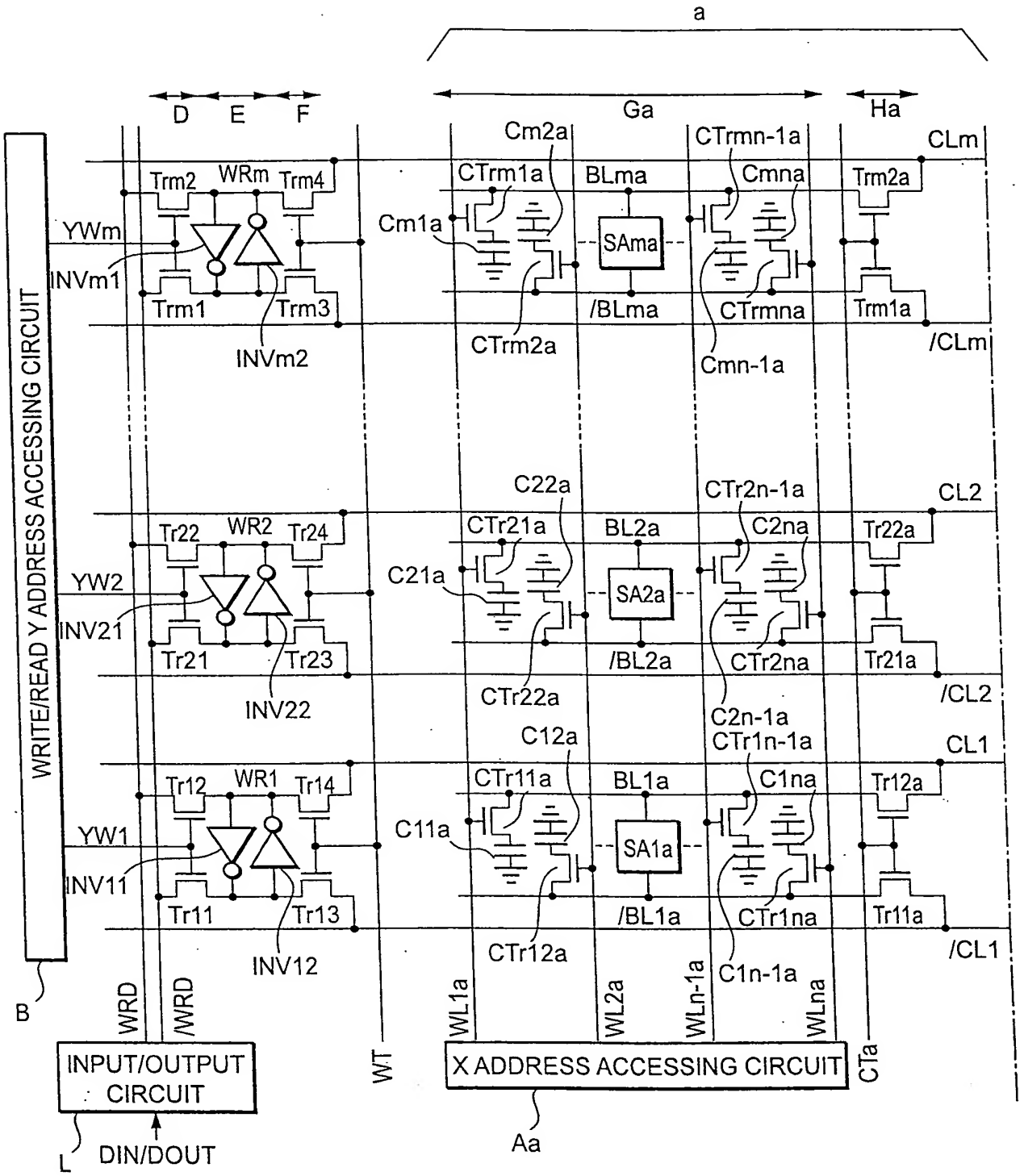
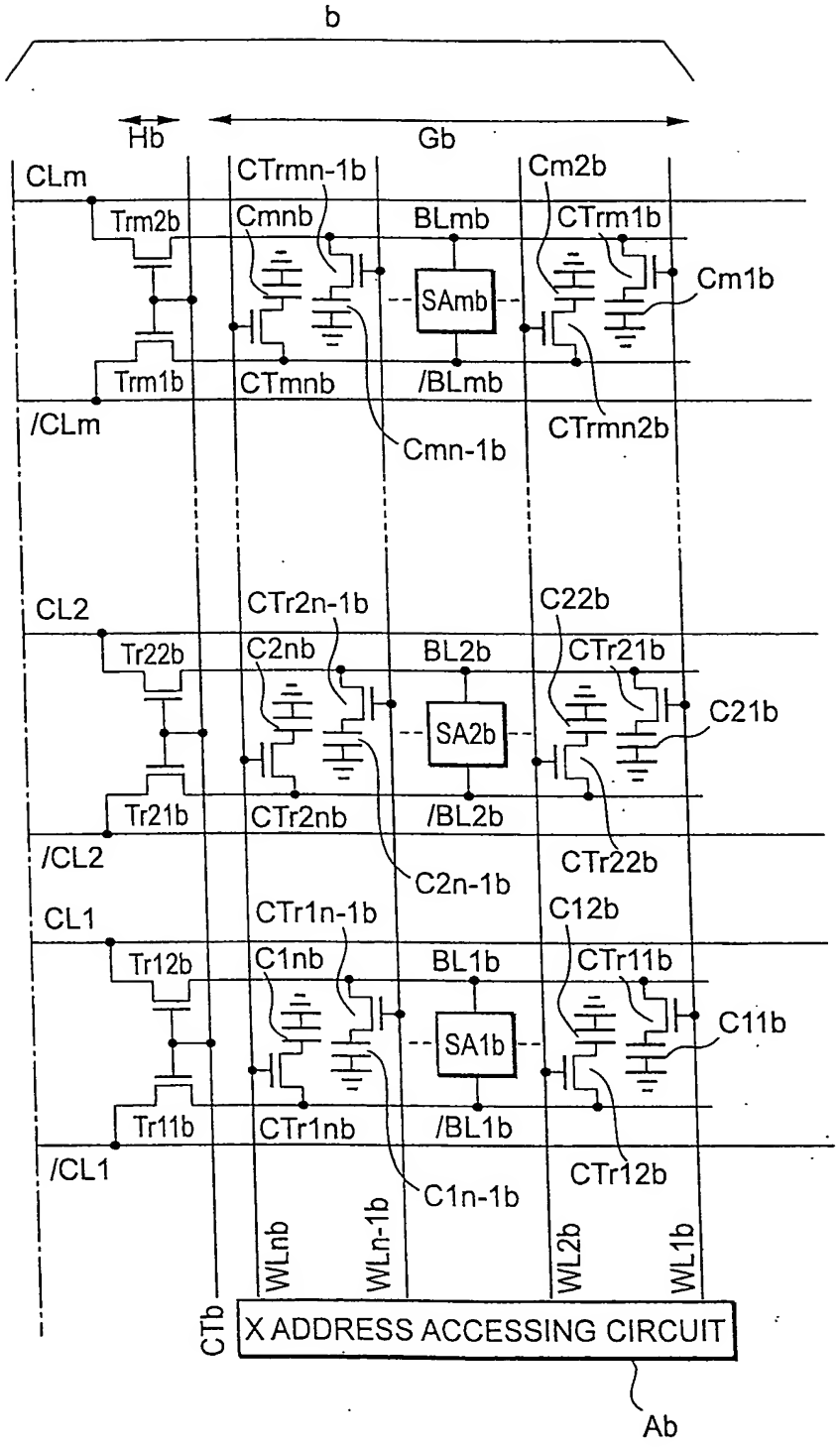

a
D
E
F
Ga
Ha
WRITE/READ Y ADDRESS ACCESSING CIRCUIT
Trm2
WRm
Trm4
YWm
INVm1
Trm1
Trm3
INVm2
Cm2a
CTrm1a
BLma
CTrmn-1a
Cmna
CLm
Trm2a
Cm1a
SAma
/BLma
CTrmna
Trm1a
/CLm
CTrm2a
Cmn-1a
C22a
CTr2n-1a
CL2
Tr22
WR2
Tr24
YW2
INV21
Tr21
Tr23
INV22
CTr21a
BL2a
C2na
Tr22a
C21a
SA2a
/BL2a
CTr2na
Tr21a
/CL2
CTr22a
C2n-1a
C12a
CTr1n-1a
CL1
Tr12
WR1
Tr14
YW1
INV11
Tr11
Tr13
INV12
CTr11a
BL1a
C1na
Tr12a
C11a
SA1a
/BL1a
CTr1na
Tr11a
/CL1
CTr12a
C1n-1a
B
WRD
/WRD
WT
WL1a
WL2a
WLn-1a
WLna
CTa
INPUT/OUTPUT CIRCUIT
X ADDRESS ACCESSING CIRCUIT
L
DIN/DOUT
Aa

FIG.11B


b
Hb
Gb
CLm
CTrmn-1b
Cm2b
Trm2b
Cmnb
BLmb
CTrm1b
Cm1b
SAmb
Trm1b
CTmnb
/BLmb
/CLm
Cmn-1b
CTrmn2b
CL2
CTr2n-1b
C22b
Tr22b
C2nb
BL2b
CTr21b
C21b
SA2b
Tr21b
CTr2nb
/BL2b
/CL2
C2n-1b
CTr22b
CL1
CTr1n-1b
C12b
Tr12b
C1nb
BL1b
CTr11b
C11b
SA1b
Tr11b
CTr1nb
/BL1b
/CL1
C1n-1b
CTr12b
WLnb
WLn-1b
WL2b
WL1b
CTb
X ADDRESS ACCESSING CIRCUIT
Ab